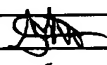
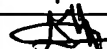


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List of Patents and Publications Statement (Use several sheets if necessary)		Applicant: Bharat, Bhushan, et al.
Page 1 of 3		Filing Date : H rewith

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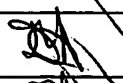


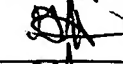

12/17/01

REFERENCE DESIGNATION			U.S. PATENT DOCUMENTS			
Examiner Initials		Document No.		Class	Sub-Class	Filing date if appropriate
	AA	5,341,322	Fettweis, et al.	364	764	5/11/92
	AB	5,270,962	Fettweis	364	766	3/11/93
	AC	4,890,127	Darley	364	786	12/26/89
	AD	5,115,408	Darley, et al.	364	754	2/5/91
	AE	5,923,579	Widigen, et al.	364	786.01	2/22/95
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	AG	5,815,420	Steiss	364	736.04	7/31/97
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	AQ	5,144,577	Linnenberg	364	769	2/27/91
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	AT	4,967,388	Tate	364	760	4/21/88

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	AV						

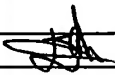
OTHER ART (Including Author, Title, Date, Pertinent Pages, etc.)

	AW	PCT International Search Report, Application No. PCT/US 00/ 42165, date of completion of the search, July 3, 2001
	AX	Cortadella J. et al.: "Evaluation of A + B = K Conditions Without Carry Propagation" IEEE Transactions on Computers, Vol. 41, No. 11, November 1992
	AY	Parhami, B.: "Comments on Evaluation of A + B = K Conditions Without Carry Propagation" IEEE Transactions on Computers, Vol. 43, No. 4, April 1994
	AZ	Duprat J. et al.: "Ecrire les nombres autrement pour calculer plus vite" Technique et Science Informatiques, Vol. 10, No. 3, 1991
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




Examiner D. H. Malzahn Date Considered 2/11/04

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Form PTO-1449 (Modified)		Priority Dock t No.: 042390.P9001		Serial No.: Not Yet Assigned			
List of Patents and Publications Statement (Use several sheets if necessary) Page 2 of 3				Applicant: Bharat, Bhushan, t al.			
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REFERENCE DESIGNATION			U.S. PATENT DOCUMENTS			
Examiner Initials	Document No.	Document No.	U.S. Patent Documents	Class	Sub-Class	Filing date if appropriate
	AA	5,754,819	Lynch et al.	395	421.08	7/28/94
	AB					
	AC					
	AD					
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No.	Document No.	Date	Country	Class	Sub-Class	Trans-lation	
	AU						
	AV						

OTHER ART (Including Author, Title, Date, Pertinent Pages, etc.)		
	AW	Lutz, D. et al.: "Early Zero Detection", International Conference on Computer Design, pp. 545-550, 1996
	AX	Lutz, D. et al.: "The Half-Adder Form and Early Branch Condition Resdolution" Arithmetic 13, pp. 266-273, 1997
	AY	Lutz, D. et al.: "Comparison of two's complement numbers" Int. J. Electronics, Vol. 80, No. 4, pp. 513-523, 1996
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Examiner <i>D.H. Malzahn</i>	Date Considered <i>2/11/04</i>
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EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

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Atty Dock t No.:
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Page 3 of 3

Applicant: Bharat, Bhushan, t al.

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
U.S. PATENT DOCUMENTS

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No.		Document No.	Date	Country	Class	Sub-Class	Trans-lation
	AU						
	AV						

OTHER ART (Including Author, Title, Date, Pertinent Pages, etc.)

	AW	Ling, H., "High-Speed Binary Adder", IBM Journal of Research and Development, Vol. 25, No. 2-3, pp. 156-166, May-June 1981
	AX	
	AY	
	AZ	
	BA	

Examiner *D H. Mulzahn*

Date Considered *2/11/04*

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Substitute for Form 1449A-PTO (Modified) (use as many sheets as necessary)		#5	Attorney Docket No.: 42390.P9001	Application Number: 10/032,026
Page 1 of 1		First Named Inventor: Bharat Bhushan, et al.		Examiner: Unassigned
		Filing Date: December 17, 2001		Art Unit: 2121 2124

U.S. PATENT DOCUMENTS

Exam. Initial*	Cite No. ¹	U.S. Patent Document		Name of Patentee or Applicant of Cited Document	Date of Publication of Cited Document MM-DD-YYYY	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number	Kind Code ² (If known)			
10/032,026		4,569,032		Lee	02-04-1986	
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OTHER ART - NO PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published	Translation ²
10/032,026		Dobberpuhl, D.W., et al., "A 200-Mhz 64b Dual-Issue CMOS Microprocessor," IEEE Journal of Solid State Circuits, Vol. 27, No.11, November 1992, pp. 1555-1567.	
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Examiner Signature	D.H. Malzahn	Date Considered	2/11/04
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